DEVELOPMENT OF ELECTRIC SCHEME FOR 4-CHANNEL LOW NOISE RAIL-TO-RAIL OPERATIONAL AMPLIFIER ARD824 BASED ON AD824 PROTOTYPE

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Abstract. Analog Devices chip AD824 is a low-power single polarity Rail to Rail in exit 4-channel operational amplifier with n-channel FET transistors at the input. Its characteristics allow to use them in various high ohmic detectors for photonics and medicine. The task was to construct an operational amplifier aRD824 that has similar performance characteristics of AD824. For this, AD824 chip and its electric scheme were analyzed, and some of its modules were produced and tested. It appeared that the production line of the producer "Integral" could not produce well FET transistors and thin layer resistors that are used in AD824, which resulted in a high percentage of damaged chips. For this, the modification of electric schemes for various modules of AD824 was proposed. Thin film resistors were proposed to be substituted by ion implantation or diffusion resistors. The input stage module got additional source repeaters. The second stage module was modified to be more symmetric. The output stage module obtained additional resistors and capacitors to achieve a frequency compensation. One FET transistor in the current reference module was substituted by other elements. The performance of modified electric schemes of modules was tested in PSpice software. Simulations of the full electric scheme for aRD824 were made and showed that it demonstrates similar characteristics as AD824 in frequency-gain and signal response tests. The targeted characteristics for aRD824 chip include low voltage noise < 4 μV for 0.1Hz to 10 Hz input, low input bias current < 15 pA, and offset voltage < 0.5 mV.

Keywords: operational amplifier, AD824, electric scheme, rail-to-rail.

Introduction

Operational amplifiers [1] with junction field effect transistors (JFET) [2-4] have been produced already for more than 50 years, even as modules and hybrid chips. This was initiated by the need to work with signals from high ohmic detectors used, for example, in photonics, medicine [5], capacitor detectors, and electret microphones. The first monolithic operation amplifiers with JFET appeared in the 70-ties (for example, uA 740, ICL8007). They had low offset parameters and could not compete with bipolar operational amplifiers. It is explained by undeveloped technology for JFET production at that time. By inspection of the processes in JFETs and by improving the production technologies in the 70-80ties, the next level operational amplifiers were produced (for example, LF 155, OP 15, AD 542). These were satisfactory amplifiers per se, yet their performance was weaker than bipolar amplifiers in respect to various parameters, for example, bias voltage. The main advantage was that JFET operational amplifiers could be produced by technologies that were present in various production lines. In the 90-ties the company Analog Devices developed technology for vertical npn and pnp transistors, which was called complementary bipolar (CB) [6]. This technology allowed to improve significantly various chip solutions, including operational amplifiers. Based on this technology, the company Analog Devices developed various operational amplifiers – AD820 (1993) [7], AD822 (1994) [8], AD823 (1995), AD824 (1995) [9]. They demonstrated extraordinary characteristics for operational amplifiers with respect to input current, noise level, good dynamics, and low current consumption. These amplifiers did not have the highest available characteristics for their individual parameters, but together they appeared to be very useful for many applications within the above-mentioned technologies, especially where low-level input current is required.

The task for developers of this research was to construct and test a 4-channel low noise rail-to-rail operation amplifier aRD824 with the specification given in Table 1, based on an initial prototype Analog Device AD824 chip [9]. AD824 is a low-power single polarity Rail to Rail in exit 4-channel operational amplifier with n-channel FET transistors at the input. The production of chips for aRD824 was planned to be realized at the production facility of JSC "Integral" in Belarus. Due to limitations and specificity of production processes in this facility, the construction of a chip that uses an electric scheme of AD824 prototype is not applicable as a high rate of damaged chips may be obtained. Therefore, a modified electric scheme of AD824 prototype was proposed that allows it to reach the expected specification.

Table 1

Planned specification of the developed operational amplifier aRD824 chip and actual specification of Analog Devices AD824 chip

Parameter	aRD824 (planned)		AD824 [9]			Units
	Minimal values	Maximal values	Minimal values	Typical	Maximal values	
Offset Voltage T_{MIN} to T_{MAX}	-0.5 -0.8	0.5 0.8	-	0.1	1.0	mV
Input Bias Current T_{MIN} to T_{MAX}	-	15 4000	-	2 300	12 4000	pA
Input Offset Current T_{MIN} to T_{MAX}	-	10 300	-	2 300	10	pA
Large Signal Voltage Gain R_L = 2 kΩ R_L = 10 kΩ R_L = 100 kΩ T_{MIN} to T_{MAX}, R_L = 100 kΩ	20 50 250 180	-	20 50 250 180	40 100 1000 400	-	$V \cdot mV^{-1}$
Output Voltage (High) I_{SOURCE} = 20 μA I_{SOURCE} = 2.5 mA	4.975 4.800	-	4.975 4.800	4.988 4.985	-	V
Output Voltage (Low) I_{SOURCE} = 20 μA I_{SOURCE} = 2.5 mA	-	25 150	-	15 120	25 150	mV
Voltage noise 0.1 Hz to 10 Hz	-	4	-	2	-	μV p-p

Materials and methods

The electric scheme of the AD824 chip was derived from its datasheet [9] and from visual observations of its physical structure. Modules of the derived electric scheme (see, for example, Fig.1 and Fig.3) were produced at "Integral" and compared with modules of AD824. It was observed that n-channel FET transistors cannot be reproduced with satisfactory good precision and results in high voltage noise. Fig.1 shows an electric scheme of a module for which the voltage V_{gs} noise is in the range 5 to 10 μV for input noise signal 0.1-10 Hz. This is about 5 times more than values for similar schemes based on npn transistors. Output current-voltage characteristic curves (Fig. 2) for FET transistors, produced at "Integral", show a wider "Ohmic region" compared to AD824 transistors. This region is characterized by lower values of transconductance g_m compared to a saturation region: $g_m = dI_d/dV_{gs}$, where dI_d – increment of a drain current I_d, and dV_{gs} – increment of a gate-source voltage V_{gs}. Thus, when the FET transistor moves toward the "Ohmic region" (when the source voltage is close to the drain voltage), a gain is reduced significantly as it is proportional to g_m. As the input stage of AD824 is similar to Fig. 1, its gain experiences the same reduction. So, when the operational amplifier input voltage *Ugs* is increased towards + *Vcc* – 2V … + *Vcc* – 1 V, its gain may drop by hundreds. For amplifiers with a high gate cut-off voltage on FET transistors, this drop is even stronger.

The technological line of "Integral" allows creation of thin film resistors, which are similar to those of AD824. But the useful output of such products is 5-10 times less than for chips, which use diffusion and ion implanted resistors. Therefore, it was decided to use diffusion [10] and ion implanted resistors [11] in the design of aRD824. Further it is shown how several modules of AD824 were modified to match requirements for aRD824 with production possibilities of the chip producer "Integral".

Modules of electric schemes of AD824 and aRD824 were simulated in PSpice software and compared among themselves. Full electric scheme of aRD824 was simulated and compared with data tables of AD824 [9].

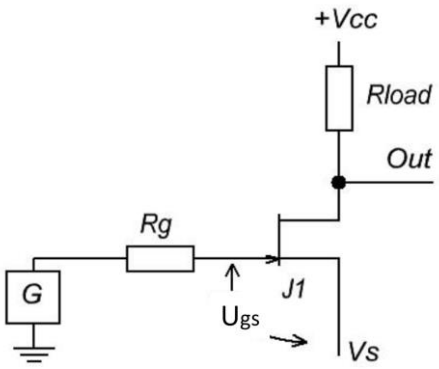

Fig. 1. **Electric scheme of module: +** *Vcc* – supply voltage; *Rg* – generator resistor; *Rload* – load resistor; J1 – FET transistor; *G* – signal generator; *Vs* – voltage on source; *Ugs* – voltage gate source

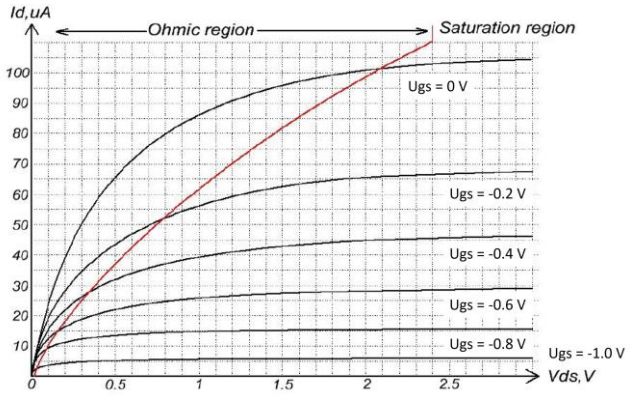

Fig. 2. **Exit current-voltage characteristics:** *Vds* – voltage drain source; *Id* – drain current; *Ugs* – voltage gate source; Red line – separation between ohmic and saturation regions for various *Ugs*.

Results and discussion

Modification of the Input stage module

Changes were proposed to an electrical scheme of the Input stage [12] of a chip. The electric scheme of the input stage of AD824 is given in Fig. 3. An electric scheme of the input stage for aRD824 is given in Fig. 4. By changing a scheme, a task was to decrease the noise in the input stage and expand the range of input signals. It was decided to include source repeaters transistors J1 and J2. This allows for decreasing the input voltage noise by more than 5 times. Meanwhile, a range of input signals at a top region of the scheme (+ *Vcc* – 2V … + *Vcc* – 1V) is increasing by the value of about V_{ref} as voltage on drains of transistors J1 and J2 (Fig.4.) is higher by *Vref* than in Fig.3.

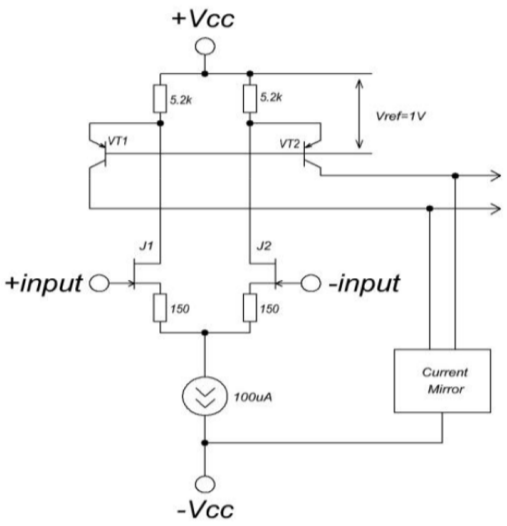

Fig. 3. **Electric scheme of an input stage module of AD824**

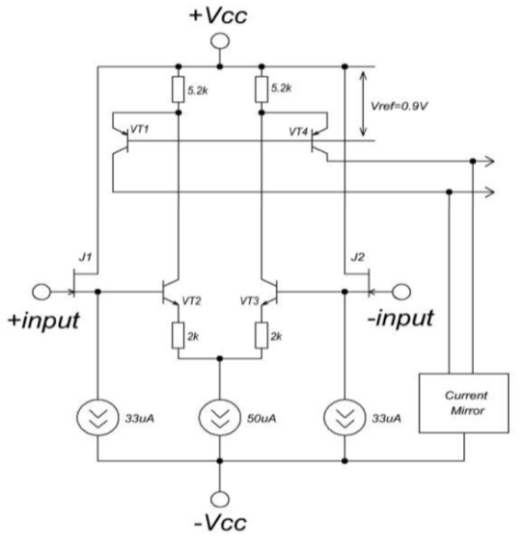

Fig. 4. **Electric scheme of an input stage module of aRD824**

The scheme in Fig. 4 has some disadvantages. First, the introduction of an additional cascade increases a phase shift and initiates a decrease in its stability. Second, the additional cascade introduces a limitation on a cutoff voltage of input transistors J1 and J2. The cutoff voltage must be below -0.9 V to -1.0 V. If not, then transistors VT2 and VT3 of the differential cascade will be closed when the input signal is close to -*Vcc*. Despite the disadvantages, the developed scheme will be introduced. Problems

with stability will be solved by changing a second stage module (Fig.6) and introducing frequency correction in an output stage module (Fig. 8).

Modification of the second stage module

Schemes for the second stage of AD824 and aRD824 are given in Fig. 5 and Fig. 6, respectively. aRD824 has a symmetric structure and, therefore, a similar time for the signal path in the upper and lower arms. Drain currents of transistors VT1 and VT2 (Fig. 6) were selected in a way to compensate base currents for medium values of β for npn and pnp transistors. In Fig. 5 the AD824 second stage module has additional signal delay created from signal transfer in the upper arm (VT1-VT3-VT2-VT4) and is compensated by the capacitor C1 that is connected in parallel. Calculations showed that signal delay in Fig. 6 is smaller than in Fig. 5 even in cases when much smaller currents are in the cascade. Thus, the scheme in Fig. 6 gives larger signal stability than the scheme in Fig. 5.

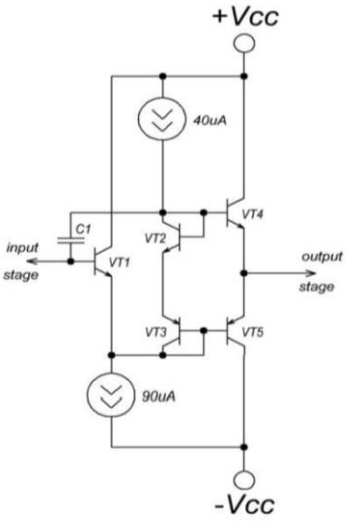

Fig. 5. **Electric scheme of a second stage module of AD824**

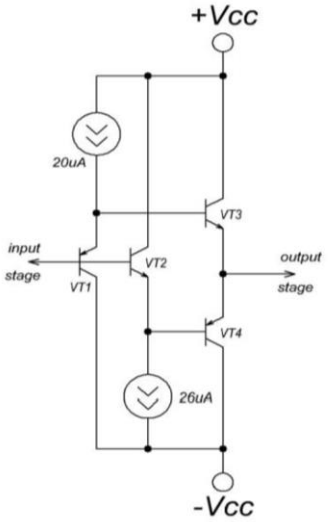

Fig. 6. **Electric scheme of a second stage module of aRD824**

Modification of the output stage module

In Fig. 7 and Fig. 8 simplified schemes for an output stage of AD824 and aRD824 are given. To compensate the phase shift initiated in the input stage by transistors VT2 and VT3 (Fig. 4), elements for phase corrections were introduced – capacitors C1 and C2, and resistors R1 and R2 (Fig. 8).

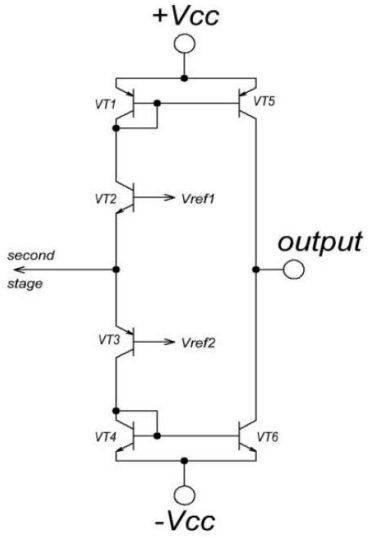

Fig. 7. **Electric scheme of an output stage module of AF824**

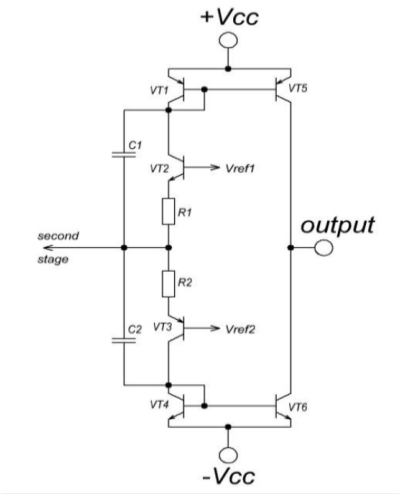

Fig. 8. **Electric scheme of an output stage module of aRD824**

Modification of the current reference module

In Fig. 9 and Fig. 10 simplified schemes for a current reference module of AD824 and aRD824 are given. In the scheme of Fig. 10, only one FET transistor J1 is used as a trigger element, which has low requirements for its quality. Current in each of 4 channels is set using pnp transistors VT10, VT11, etc. This is approximately equal to the sum of the current that passes resistors R3 and R4. The current through the resistor R3 has a positive temperature coefficient, but through R4 – a negative temperature coefficient. Additionally, the resistance of diffusion or ion-implanted resistors is dependent on temperature. Values for R3 and R4 were selected to keep the current in VT10, VT11, etc., the same for the temperature region -40 ºC… 85 ºC. The exact value of the reference current is set by trimmable resistors connected in series to R6, R7, … The sum of the current drift within the temperature region -40 ºC… 85 ºC for the whole spectra of voltages has to be below 5 - 10%. If there is a need to change a thin film resistor to ion-implanted or diffusion, the effect of temperature was estimated to be minimal, and no need will appear to adjust this electric scheme.

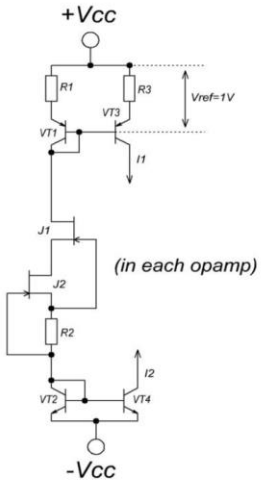

Fig. 9. **Electric scheme of a current reference module of AD824**

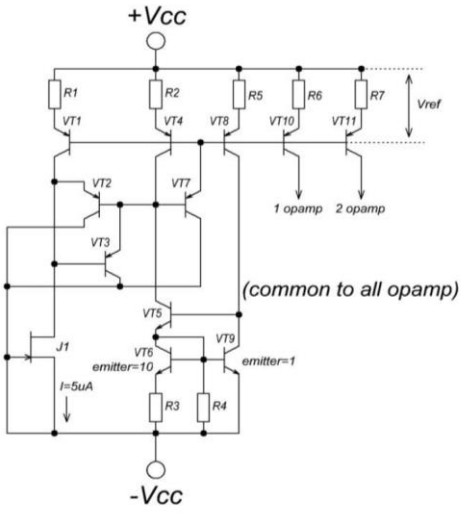

Fig. 10. **Electric scheme of a current reference module of aRD824**

*Simulation results of aRD*824

The electric scheme of aRD824 was simulated in PSpice software. Results were compared to characteristics of AD824 as reported in their data sheets [9]. In Fig. 11 gain graph for various signal frequencies in no load case is given. In Fig. 12 a simulated gain graph of aRD824 is given, when there is no load, + *Vcc* = + 5V, -*Vcc* = 0 V, and *Vinp* = 1 μV. It can be seen that the frequency-gain graphs for AD824 and aRD824 are much similar.

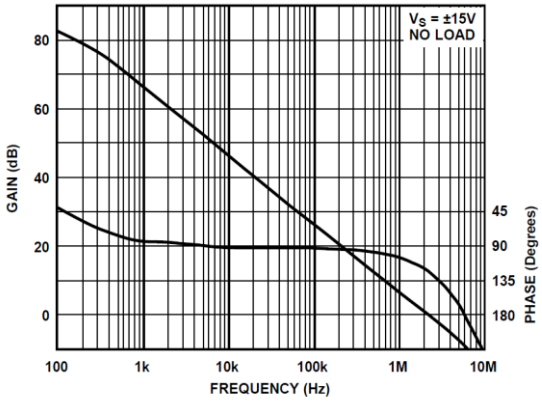

Fig. 11. **Gain (dB) dependence on signal frequency with no load of AD824 [9]**

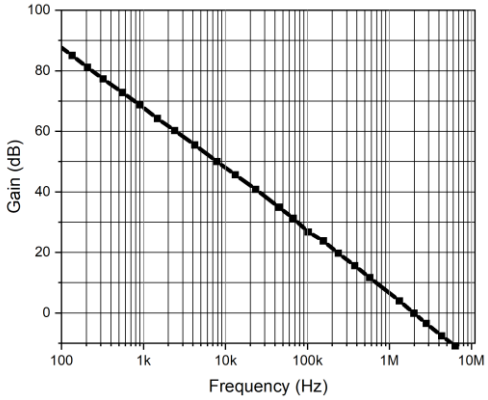

Fig. 12. **Simulated gain (dB) dependence on signal frequency with no load of aRD824**

In Fig. 13 a small signal response graph of AD824 is given when no load is applied and *Vs* = 5 V. In Fig. 14 a small signal response graph of aRD824 is given when no load is applied, + *Vcc* = + 5V, and -*Vcc* = 0 V. It can be seen that both graphs are much similar.

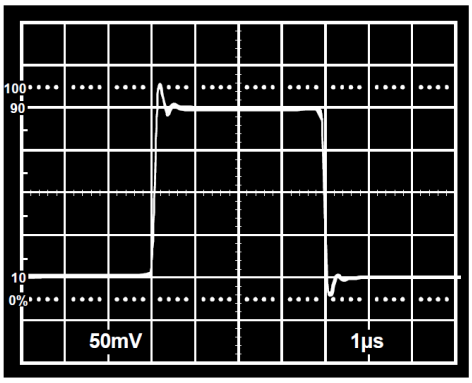

Fig. 13. **Small signal response, *Vs* = 5 V, no load, AD824 [9]**

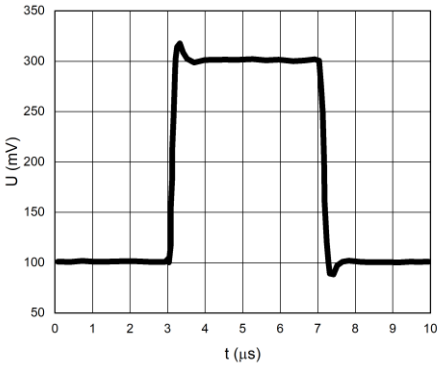

Fig. 14. **Small signal response with no load of aRD824**

Conclusions

The task of the research was to design, construct and test a 4-channel low noise rail-to-rail operation amplifier aRD824 with the specification given in Table 1, based on an initial prototype Analog Device AD824 chip. Due to limitations and specificity of production processes in the production facility "Integral", the construction of a chip that is an implementation of an electric scheme of AD824 prototype is not applicable as a high rate of damaged chips may be obtained. Therefore, a modified electric scheme of AD824 prototype was proposed that allows it to reach the expected specification. Thin-film resistors were proposed to be substituted for ion implantation or diffusion resistors. The input stage module got additional source repeaters (Fig. 4). The second stage module was modified to be more symmetric (Fig. 6). The output stage module obtained additional resistors and capacitors to achieve a frequency compensation (Fig. 8). One FET transistor in the current reference module was substituted by other elements (Fig. 10). The performance of the modified electric schemes of modules was tested in PSpice software. Simulations of the full electric scheme for aRD824 were made and showed that it demonstrates similar characteristics as AD824 in frequency-gain (Fig. 11 and Fig. 12) and signal response (Fig. 13 and Fig. 14) tests.

The conclusion can be made that the developed electric scheme of aRD824 can be used as an alternative to AD824 and is expected to reach similar performance characteristics. Yet, the actual performance of aRD824 will be seen only when its chip is produced and full tests on it will be made.

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Author contributions:

Conceptualization, S.R. and M. L.; methodology, S.R., M.L. and D.K.; software, D.K.; validation, S.R.; formal analysis, D.K., S. R., M.L. and A.A.; investigation, D.K. and S. R.; data curation, D.K., S.R. and A.A.; writing - original draft preparation, A.A.; writing - review and editing, A.A., S. R. and D. K.; visualization, D.K. and A.A.; project administration, M.L.; funding acquisition, M.L. All authors have read and agreed to the published version of the manuscript.

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